APPLICATION NOTE

UNDERSTANDING POWER FACTOR

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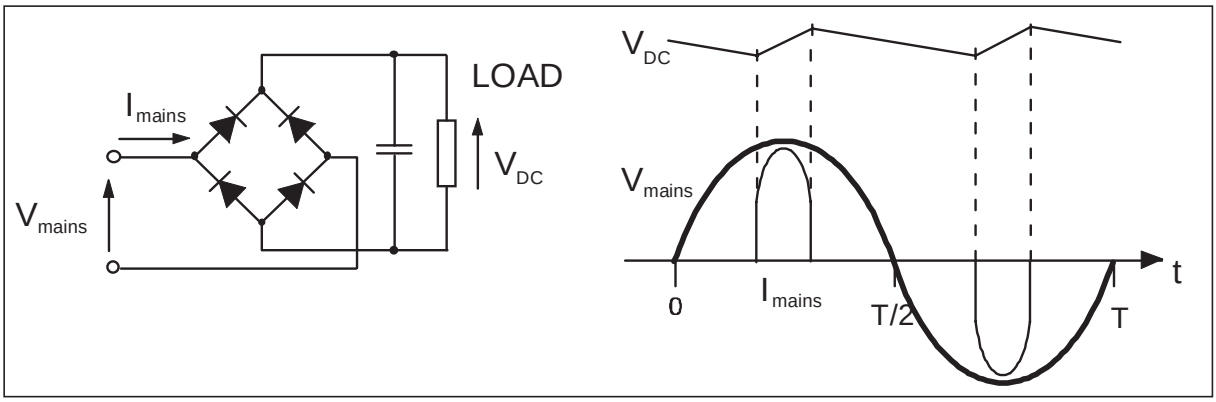
1. INTRODUCTION

The majority of electronics designers do not worry about Power Factor (PF); PF is something that you learnt one day at school in your “electrotechnics course” as being the cos of φ, the phase angle between the voltage and current waveforms. However, this conventional definition is only valid when considering ideal sinusoidal signals for both current and voltage waveforms, and in reality most off-line power supplies draw a non-sinusoidal current.

Many off-line systems will typically have a front end section consisting of a rectifier bridge and an input filter capacitor, which act as a peak detector - see figure 1. A current flows to charge the capacitor only when the instantaneous AC voltage exceeds the voltage of the capacitor. A single phase off-line supply draws a current pulse during a small fraction of the half-cycle duration. Between those current peaks, the load draws the energy stored in the input capacitor. The phase lag φ and also the harmonic content of the pulsed current waveform produce additional RMS currents, affecting the real power available from the mains. So Power Factor is much more than cos φ!

The P.F. value measures how much the mains efficiency is affected by both the phase lag φ and the harmonic content of the input current. In this context, the European Standard EN 60555 only defines the limit of current harmonics in mains supplied equipment.

Figure 1: Full-Wave Rectifier



2. THEORETICAL MEANING

The Power Factor is defined by:

$$P.F. = \frac{P}{S} = \frac{\text{REAL POWER}}{\text{APPARENT POWER}}$$

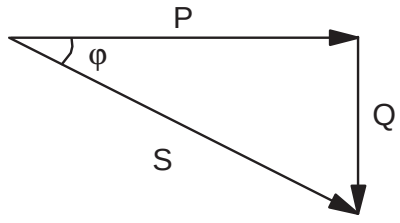
2.1 Ideal sinusoidal signals

For ideal sinusoidal voltage and current waveforms, if there is a phase difference φ between the voltage and current waveforms, the total apparent power can be modelled as being composed of two components: one in phase with the input voltage, and the other 90° out of phase (in quadrature) with it - see figure 2.

Then by definition,

$$P.F. = \frac{P}{S} = \cos \varphi$$

Figure 2: Power vectors of ideal sinusoidal signals



$P = V_{RMS} . I_{RMS} \cos \varphi$:	In-Phase or Real Power
$Q = V_{RMS} . I_{RMS} \sin \varphi$:	Reactive or Quadrative Power
$S = V_{RMS} . I_{RMS}$:	Total Apparent Power

2.2 Non-ideal sinusoidal current

Assuming that the mains voltage is an ideal sinusoidal voltage waveform, its RMS value is:

$$V_{RMS} = \frac{V_{peak}}{2}$$

If the current has been distorted in some way (for example as in figure 1) into a periodic non-sinusoidal waveform, applying a Fourier transform gives:

$$I_{RMS(total)} = \sqrt{I_0 + I^2_{1RMS} + I^2_{2RMS} + ... + I^2_{nRMS}}$$

where I_0 is the DC component of the current, I_{1RMS} the fundamental of the RMS current (that is the component at the frequency of the voltage input) and I_{2RMS} ... I_{nRMS} are the harmonics created by the distortion.

For a pure AC signal, there is no DC component and so $I_0 = 0$.

The fundamental of the RMS current can be modelled as in section 2.1 above as an in-phase component I_{1RMSP} and a quadrature component I_{1RMSQ}, and so the RMS current can be expressed as:

$$I_{RMS(total)} = \sqrt{I_0 + I^2_{1RMS\,P} + I^2_{1RMS\,Q} + \sum_{n=2}^{\infty} I^2_{nRMS}}$$

Then, the Real Power is given by the RMS voltage multiplied by the in-phase current:

$$P = V_{RMS} . I_{1RMS\,P}$$

As φ_1 is the displacement angle between the input voltage and the in-phase component of the fundamental current:

$$I_{1RMS\,P} = I_{1RMS} \cos \varphi_1$$

so

$$P = V_{RMS} \cdot I_{RMS} \cos \varphi_1$$

As the total apparent power is given by:

$$S = V_{RMS} \cdot I_{RMS\ total}$$

the Power Factor can be calculated as :

$$P.F. = \frac{P}{S} = \frac{I_{1\,RMS} \cdot \cos \varphi_1}{I_{RMS\ (total)}}$$

If the phase angle between I_{1RMS} and $I_{RMS(total)}$ is defined as θ:

$$\cos \theta = \frac{I_{1\,RMS}}{I_{RMS\ (total)}}$$

θ is linked to the harmonic content of the current; as the harmonic content of $I_{RMS(total)}$ approaches zero, θ approaches 0 and $\cos \theta$ approaches 1.

2.3 Summary

Finally then, the Power Factor can be expressed as:

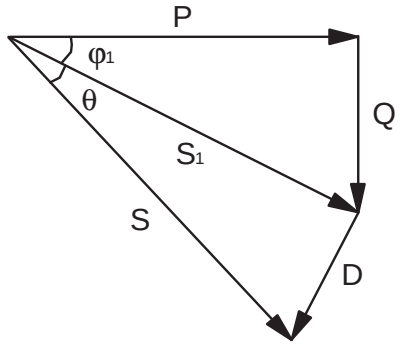
$$\mathbf{P.F. = \cos \theta \cdot \cos \varphi_1}$$

and the representation of the power vectors becomes that shown in figure 3.

φ_1 is the "conventional" displacement angle (phase lag) between the voltage and the fundamental component of the current, while θ is the distortion angle caused by the harmonic content of the current.

Both the reactive power, Q, and the distortion power, D, produce extra RMS currents, giving additional losses and reducing the efficiency of the mains supply network.

Figure 3: Power vectors with non-sinusoidal signals.



P = Real Power
$= V_{RMS} \cdot I_{RMS} \cdot \cos \varphi$

Q = Reactive Power
$= V_{RMS} \cdot I_{RMS} \cdot \sin \varphi$

S_1 = Apparent Fundamental Power
$= V_{RMS} \cdot I_{1RMS}$

D = Distortion Power
$= V_{RMS} \cdot \sqrt{\sum_{n=2}^{\infty} I^2_{nRMS}}$

S = TOTAL APPARENT POWER
$= V_{RMS} \cdot I_{RMS\ (total)}$

Improving the Power Factor means reducing both elements:

$$\varphi_1 \rightarrow 0 \quad \text{means COS } \varphi_1 \rightarrow 1:$$

reduction of the phase lag between I and V,

$$\theta \rightarrow 0 \quad \text{means COS } \theta \rightarrow 1:$$

reduction of harmonic content of I.

3. PRACTICAL IMPLICATIONS OF POWER FACTOR

3.1 Benefits of reduced Power Factor

Both the user and the electricity supply company can benefit from a reduction in Power Factor. Adding a PFC also reduces the component costs in a downstream converter.

3.1.1 Benefits to the user

At the minimum line voltage ($85V_{AC}$), a standard $115V_{AC}$ wall socket should be able to deliver the nominal 15A to a common load. However, an SMPS without a Power Factor Corrector (PFC), which will typically have a Power Factor of 0.6, reduces the available current to around 9A.

As an example, a single wall socket will supply four 280W computers equipped with PFCs, but only two without.

3.1.2 Benefits to the distribution company

Both the reactive power Q and the distortion power D give rise to extra RMS currents, significantly reducing the efficiency of the mains supply network. This means that the copper distribution wires must be thicker than would otherwise be necessary.

Delivering power at frequencies other than the line frequency (ie the distortion power D) also causes difficulties. The distortion disturbs the zero voltage crossing detection systems, and generates overcurrent in the neutral line and resonant overvoltages.

In Europe, the standard EN 60555 and the international project IEC 555-2 limit the harmonic content of the current of mains supplied equipment.

3.1.3 Reduction of component costs in the downstream converter

For the same output power capability, a conventional converter using an input mains voltage doubler has primary RMS current 1.8 times higher than one employing a PFC regulator. Consequently, if a PFC is used in a system using Power MOSFET switches, the on-resistance ($R_{DS(ON)}$) of the switches can be up to three times higher than in a system without PFC, allowing significantly cheaper parts to be used.

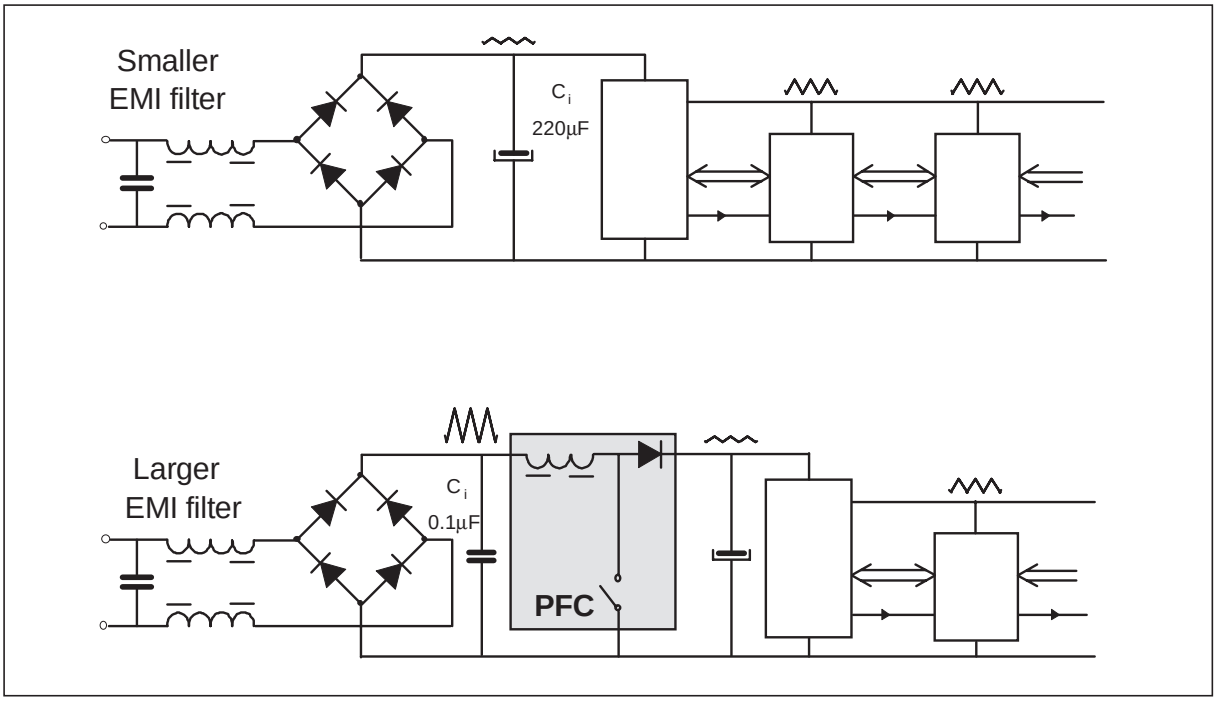
The size of the converter transformer can be reduced not only because the thickness of the windings is smaller, but also because of the regulation of the DC bulk voltage delivered by the PFC pre-regulator.

The PFC provides an automatic mains selection on a wide range of voltages from $85V_{AC}$ up to $265V_{AC}$. Compared to the conventional doubler front-end section the same hold-up time can be achieved with a bulk storage capacitor 6 times smaller. For example, to achieve a 10ms hold-up time, a 100W converter in doubler operation requires a series combination of two 440µF capacitors without a PFC, but only a single 130µF with.

3.2 RFI filter

However, the size and cost optimisation of the PFC has to take the RFI filter into consideration. A PFC circuit generates more high frequency interference to the mains than a conventional rectifier front-end - see figure 4. Thus the use of a PFC means that additional filtering is required. For this reason, modulation techniques and mode of operation for the PFC have to be carefully adapted to the requirements of the application.

Figure 4: SMPS with (a) conventional rectifier front-end, and (b) PFC front-end.



4. CONCLUSIONS

For new designs, SMPS designers will have to take into account the IEC 555-2 standard. In practice, this will require the use of a PFC on the front end of much mains supplied equipment. The additional cost of the PFC is compensated by the significant reduction in the cost of components for the downstream converter. The PFC also provides additional functions such as automatic mains voltage selection and constant output voltage.